Mayank Neupane

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EDUCATION

York University May 2027 (Expected)
Bachelor of Science, Computer Engineering

PROJECTS

RISC-V CPU (RV32I) Jan. 2026 - Present

- Built a 32-bit 5-stage pipelined RISC-V CPU in System Verilog with Fetch, Decode, Execute, Memory & Write-Back stages.
- Implemented hazard and branch handling with stalling, flushing, forwarding, and PC/control-flow logic.
- Integrated and debugged the datapath and control path including ALU, register file, immediate generation, and load/store memory interface using waveform analysis.
- Developed automated verification/regression testing with SystemVerilog, Python, and ModelSim/Verilator, validating execution with compiled C benchmarks loaded as ELF/binary images.

FPGA-Based Wireless Vehicle Control System Nov. 2025 – Dec. 2025

- Designed and deployed an FPGA-controlled vehicle using RTL combinational/sequential logic for real-time motor control, sensor processing, and wireless command handling.
- Implemented wireless communication between the FPGA and ESP32, enabling remote command transmission and responsive vehicle control.
- Integrated HC-SR04 ultrasonic sensing for obstacle avoidance and ADXL345 accelerometer input for tilt-based PWM speed control, translating real-world sensor data into dynamic motion behavior.
- Built a transistor-based NPN isolation stage for safe GPIO-to-L298N interfacing, and completed full hardware assembly through soldering and a custom 3D-printed enclosure for reliable operation.

CRUD Based System July 2025 – Aug. 2025

- Developed an in-memory database system in C supporting CRUD operations, sorting, record history tracking, and persistent storage using structs, pointers, and dynamic memory allocation.
- Implemented robust memory management with safe allocation/deallocation routines to prevent leaks and ensure reliable handling of growing datasets.
- Built an automated regression test harness with stdin redirection and validation checks, including binary file I/O testing to ensure data integrity.

EXPERIENCE

Supervisor for Ride Department | *Centreville Amusement Park* May 2022 – Sept. 2025

- Led daily operations of mechanical/electrical rides, ensuring full TSSA safety compliance and reliable uptime across multiple attractions to improve guest flow and Safety.
- Supervised and scheduled 35+ ride operators, training new staff & resolving operational issues to reduce downtime

Skills

- Programming: C, C++, Python, Java, SQL, Bash, SystemVerilog/Verilog, HTML/CSS
- Hardware: FPGA Design, RTL Development, Embedded Systems, Arduino, Sensor Integration, Hardware Debugging
- Computer Architecture: RV32I RISC-V, Pipelining, Datapath/Control Design, Verification, Waveform Debugging
- Tools: Git/GitHub, ModelSim, Verilator, MATLAB, LTSpice, PSpice, KiCad, Power BI, Figma
- Engineering & Professional: Digital Logic Design, Circuit Simulation, OOP, Testbench Development, Regression Testing, Root Cause Analysis, Documentation, Communication, Teamwork, Project Planning

Leadership

Judge & Mentor | Unhack by Lassonde School of Engineering Sept. 2023 & 2024

Awards & Honours

Rain It In 2025 – Top 5 Finalist, Rain It In
UnHack 2023 – Top 8 Finalist, York University
Employee of the Season (×2), Centreville Amusement Park — 2023 & 2024